

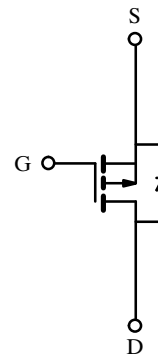
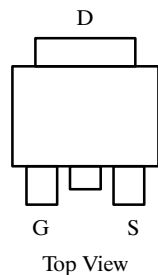
P-Channel Enhancement-Mode Transistor

175°C Maximum Junction Temperature

Product Summary

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D^a (A)
-60	0.28	-10

DPAK (TO-252)



P-Channel MOSFET

Absolute Maximum Ratings ($T_C = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V_{DS}	-60	V	
Gate-Source Voltage	V_{GS}	± 20		
Continuous Drain Current ^b	I_D	$T_C = 25^\circ\text{C}$	-10	A
		$T_C = 100^\circ\text{C}$	-5.7	
Pulsed Drain Current (maximum current limited by package)	I_{DM}	-16		
Maximum Power Dissipation	P_D	$T_C = 25^\circ\text{C}$	42	W
		$T_A = 25^\circ\text{C}$	2.0 ^b	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 175	$^\circ\text{C}$	

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Junction-to-Ambient Free Air ^b	R_{thJA}	60	$^\circ\text{C}/\text{W}$
Junction-to-Case	R_{thJC}	3.0	

Notes:

- Calculated Rating for $T_C = 25^\circ\text{C}$, for comparison purposes only. This cannot be used as continuous rating (see Absolute Maximum Ratings and Typical Characteristics).
- When mounted on 1" square PCB (FR-4 material).

SMD10P06

Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-60			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-2.0		-4.0	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -48\text{ V}, V_{GS} = 0\text{ V}$			-1	μA
		$V_{DS} = -48\text{ V}, V_{GS} = 0\text{ V}, T_J = 125^\circ\text{C}$			-250	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} = -5\text{ V}, V_{GS} = -10\text{ V}$	-10			A
Drain-Source On-State Resistance ^b	$r_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -3.0\text{ A}$			0.28	Ω
Forward Transconductance ^b	g_{fs}	$V_{DS} = -10\text{ V}, I_D = -5.7\text{ A}$	2.3			S
Dynamic^a						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = -25\text{ V}, f = 1\text{ MHz}$				pF
Output Capacitance	C_{oss}					
Reverse Transfer Capacitance	C_{rss}					
Total Gate Charge ^c	Q_g	$V_{DS} = -48\text{ V}, V_{GS} = -10\text{ V}, I_D = -9.7\text{ A}$			19	nC
Gate-Source Charge ^c	Q_{gs}					
Gate-Drain Charge ^c	Q_{gd}					
Turn-On Delay Time ^c	$t_{d(on)}$	$V_{DD} = -30\text{ V}, R_L = 3\ \Omega$ $I_D \cong -10\text{ A}, V_{GEN} = -10\text{ V}, R_G = 25\ \Omega$				ns
Rise Time ^c	t_r					
Turn-Off Delay Time ^c	$t_{d(off)}$					
Fall Time ^c	t_f					
Source-Drain Diode Ratings and Characteristics						
Continuous Current	I_S	$T_C = 25^\circ\text{C}$			-2.0	A
Pulsed Current	I_{SM}				-16	
Forward Voltage ^b	V_{SD}	$I_F = 2.0\text{ A}, V_{GS} = 0\text{ V}$			-1.2	V
Reverse Recovery Time	t_{rr}	$I_F = 2.0\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$				ns
Reverse Recovery Charge	Q_{rr}					μC

Notes:

- For design aid only; not subject to production testing.
- Pulse test; pulse width duty cycle.
- Independent of operating temperature.